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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
FOTAKIS, ARISTOCRATIS	
ART UNIT	**PAPER NUMBER**
2611	

MAIL DATE	DELIVERY MODE
05/31/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/757,633	DEMIR ET AL.	
	Examiner	Art Unit	
	Aristocratis Fotakis	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 January 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01/14/2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1,8 and 15 are rejected under 35 U.S.C. 102(e) as being anticipated by Li et al (US 7,061,994).

Li teaches of a receiver (Fig.2, Col 3, Lines 43 – 44) for receiving and processing a wireless communication signal, the receiver comprising: (a) at least one demodulator (multipliers #110, #112, local oscillator #106, phase shifting device #108, Fig.2, Col 3, Lines 41 – 49), which outputs analog real (in-phase, Fig.2) and imaginary (quadrature, Fig.2) signal components on real and imaginary signal paths, respectively, in response to receiving the communication signal; (b) an analog to digital converter (ADC) (#118, #120, Fig.2) coupled to the real and imaginary signal paths for receiving the analog real and imaginary signal components and outputting respective digital real (I_1, Fig.2) and imaginary signal (Q_1, Fig.2) components (Col 4, Lines 16 – 28); and (c) a digital cross-talk compensation module (I/Q Imbalance Correction Device, #102, Fig.2)

in communication with the ADC, wherein the digital cross-talk compensation module receives the digital real (I_1, Fig.2) and imaginary signal (Q_1, Fig.2) components, estimates cross-talk interference (*phase and amplitude correction*, Col 3, Lines 19 – 31) on the real signal component resulting from energy from the imaginary signal component being induced into the real signal path (IQ imbalance), estimates cross-talk interference (Col 3, Lines 19 – 31) on the imaginary signal component resulting from energy from the real signal component being induced into the imaginary signal path (IQ imbalance) and outputs digital real (I_2, Fig.2) and imaginary cross-talk compensated signal (Q_2, Fig.2) components (Col 4, Lines 28 – 40).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.

4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 2, 9 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Li in view of Cope et al (US 2005/0157813).

Li teaches all of the limitations of claim 1, 8 and 16 as well as a real signal path for receiving the digital real signal component (I_1, Fig.2); an imaginary signal path for receiving the digital imaginary signal component (Q_1, Fig.2); a first adder for adding a real cross-talk compensation signal (xI_1 or xQ_1, Col 5, Lines 17 - 25) to the digital real signal component (I_1 or Q_1); and (vi) a second adder for adding an imaginary cross-talk compensation signal (xQ_1 or xI_1, Col 5, Lines 17 - 25) to the delayed digital imaginary signal component (Q_1 or I_1). However, Li does not teach of a first and second delay delay unit.

Cope teaches of methods and apparatus for signal distortion correction (title of invention). Cope uses a digital delay in parallel with the predistortion processing (#14, Fig.2a). This delay (#32) has unity gain and serves to time-align the linear signal with the error signal at the summing junction (#34).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have inserted a delay unit in the real/imaginary path so that the output from the delay unit would be time-aligned with the real/imaginary cross-talk compensation signal at the input of the adding units.

Claims 3, 10 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Li and Cope as applied to claims 2, 9 and 16 above, and further in view of Churchill et al. (US 3,950,750).

Li and Cope teach all the limitations of claims 2, 9 and 16. Li further teaches of a coefficient updating device (#128, Fig.2) for controlling the I/Q imbalance compensation module (#126, Fig,2) (Col 4, Lines 41 – 55). However, Li does not teach of the controller communicating with the ADC.

Churchill teach of a method and apparatus for correcting amplitude and phase imbalances between the "in phase" and "quadrature" channels of a digital signal processor by determining a correction coefficient from a test signal periodically introduced into the quadrature phase detector of a radar system (Abstract, Lines 1 – 6). A timing and control signal generator (#24, Fig.1) is used to produce a series of pulses at a frequency of 5 MHZ ("C.P./2.", Fig.1) coupled to A/D converters (36_1, 36_2, Fig. 1) so

that the analog signals applied to such converters are digitized at a 5 MHZ rate (Col 3, Lines 49 – 59). The timing and control signal generator also provides an enabling signal on a line marked "T," such signal being used by the compensator (#38)(Col 4, Lines 55 – 56).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have used a controller that would communicate on both the ADC and the compensator to maintain the synchronization between the real and imaginary components.

Claims 4, 6, 11, 13, 18 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Li in view of Pelchat et al (US 4,220,923).

Li teaches all the limitations of claim 1, 8 and 15 as well as a real or imaginary signal path for receiving the digital real or imaginary signal component as discussed above. However, Li does not specifically teach how the real or imaginary cross-talk compensation signal is been produced.

Pelchat teaches a system for an adaptive interference reduction system for crosstalk cancellation in a dual polarization system (title of invention). Pelchat teaches of a system wherein the digital cross-talk compensation module comprises (Fig.3): (i) a real (#10, vertical signal, Fig.1 and 3) or imaginary (#12, horizontal signal, Fig.1 and 3, Col 3, Lines 5 – 20) signal path for receiving the real or imaginary signal component; (ii) a delay unit (#110, #112, Fig.3) coupled to the real (#10) or imaginary (#12) signal path

for receiving the real signal component and outputting the real signal component (#128) after a predetermined delay period expires (Col 7, Lines 6 – 11); (iii) an adder (#120, Fig.3) coupled to the real or imaginary signal path and to the delay unit (as shown in Fig.2), the adder for adding a negative value (negative terminal) of the digital real signal component to the delayed digital real signal component output by the delay unit to generate a first resulting signal (Col 7, Lines 19 – 26); and (iv) a multiplier coupled to the adder (#120, Fig.3) for multiplying the first resulting signal with a compensation signal having a predetermined value (*weight*) to generate a second resulting signal (output from weighting device #124) used for adjusting the real or imaginary signal component to compensate for distortion (Col 4, Lines 2 – 5) due to the occurrence of cross-talk between the analog real and imaginary signal components (weighting device, #124, Fig.3, Col 7, Lines 27 – 29, Fig. 1 - 3).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have used the apparatus of Pelchat to produce the real or imaginary cross-talk compensation signal by the use of delay units to produce echoes, an adder to approximate a filter and a weighting device to produce a weighted and phase adjusted output from the filter to compensate crosstalk on the real or imaginary component.

Claims 5, 7, 12, 14, 19 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Li and Pelchat as applied to claims 4, 9 and 16 above, and further in view of Churchill et al. (US 3,950,750).

Li and Pelchat teach all the limitations of claims 4, 6, 11, 13, 18 and 20. Li further teaches of a coefficient-updating device (#128, Fig.2) for controlling the I/Q imbalance compensation module (#126, Fig. 2) (Col 4, Lines 41 – 55). However, Li does not teach of the controller communicating with the ADC.

Churchill teach of a method and apparatus for correcting amplitude and phase imbalances between the "in phase" and "quadrature" channels of a digital signal processor by determining a correction coefficient from a test signal periodically introduced into the quadrature phase detector of a radar system (Abstract, Lines 1 – 6). A timing and control signal generator (#24, Fig.1) is used to produce a series of pulses at a frequency of 5 MHZ ("C.P./2.", Fig.1) coupled to A/D converters (36_1, 36_2, Fig. 1) so that the analog signals applied to such converters are digitized at a 5 MHZ rate (Col 3, Lines 49 – 59). The timing and control signal generator also provides an enabling signal on a line marked "T," such signal being used by the compensator (#38)(Col 4, Lines 55 – 56).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have used a controller that would communicate on both the ADC and the compensator to maintain the synchronization between the real and imaginary components.

Response to Arguments

Applicant's arguments filed on April 17th, 2007 have been fully considered but they are not persuasive.

The Applicant submits that Li fails to teach or suggest that the IQ imbalance correction device 102 estimates the crosstalk interference caused by the real I and imaginary Q signal components.

The Examiner disagrees. Li teaches of an IQ imbalance compensation device for correcting the phase and amplitude imbalances caused by the I and Q signal components. The IQ imbalance is caused by crosstalk interference caused by each of the I and Q components. In other words, IQ imbalance is the equivalent of IQ crosstalk. This is clearly mentioned by Wright et al (US 2002/0044014) in Paragraph 0163, Lines 9 – 12, where "IQ crosstalk (IQ phase and amplitude imbalance)."

The amended claims 1,8 and 15 add the limitation as recited in the claims "estimates cross-talk interference on the real signal component resulting from energy from the imaginary signal component being induced into the real signal path, estimates cross-talk interference on the imaginary signal component resulting from energy from the real signal component being induced into the imaginary signal path". This is the definition of IQ imbalance/crosstalk interference as defined by the applicant in the background in paragraph 0007.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aristocratis Fotakis whose telephone number is (571) 270-1206. The examiner can normally be reached on Monday - Thursday 7 - 5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh Fan can be reached on (571) 272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AF

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SUPERVISORY PATENT EXAMINER